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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/593,765	06/14/2000	Hisashi Ohtani	0756-2149	8038

7590

08/26/2002

ROBINSON INTELLECTUAL PROPERTY LAW OFFICE  
PMB 955  
21010 SOUTHBANK STREET  
POTOMAC FALLS, VA 20165

EXAMINER

NGUYEN, CUONG QUANG

ART UNIT

PAPER NUMBER

2811

DATE MAILED: 08/26/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/593,765

Applicant(s)

OHTANI ET AL.

Examiner

Cuong Q Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☒ Responsive to communication(s) filed on 16 July 2002.

2a) ☐ This action is FINAL.

2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4) ☒ Claim(s) 1-52 is/are pending in the application.

4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.

5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.

6) ☒ Claim(s) 1-52 is/are rejected.

7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.

8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a) ☐ All b) ☐ Some \* c) ☐ None of:

1. ☐ Certified copies of the priority documents have been received.

2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.

3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_.

4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: \_\_\_\_\_.

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## **DETAILED ACTION**

### ***Request for Continued Examination***

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 07/16/02 has been entered. An action on the RCE follows.

### ***Claim Rejections - 35 U.S.C. § 103***

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1-4, 6-11, 13-18, 20-26, 28-30, 48- 51, are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Hsieh (US 5,153,142) in view of Tran et al. (US 5,273,910).

Hsieh discloses a semiconductor device comprising: a doped polysilicon layer (14) formed on a surface of an insulating layer (12), the polysilicon layer including

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source/drain regions, and a channel region in therebetween; a gate insulating film (16) formed on the poly silicon layer; a gate electrode (18) formed on the gate insulating film; a first insulating film (20, a silicon oxide layer) covering at least semiconductor layer and gate electrode except for contact holes opened therein; an electrode (32, an aluminum layer) formed over the second insulating film and connected to one of source/drain regions; a transparent pixel electrode (30, an ITO layer) formed over the second insulating film, wherein the pixel electrode electrically connected to the electrode and is located under the electrode. See Hsieh's Fig.8.

Hsieh does not teach that the layer (14) is a single crystal silicon layer which includes a first impurity region, a second impurity region, and a channel region in therebetween; a second insulating film of a polyimide organic resin layer formed between the electrode, pixel electrode and the first insulating film.

Tran discloses a semiconductor device comprising: a semiconductor layer (42) can be formed of a single crystal silicon or a polysilicon layer on a surface of an insulating layer (51), the semiconductor including a first impurity region (45), a second impurity region (46), and a channel region in therebetween; a gate insulating film (43) formed on the semiconductor layer; a gate electrode (49) formed on the gate insulating film; a first insulating film (a planarization layer 53) formed over the insulating surface, semiconductor layer, gate insulating film and gate electrode; the planarization layer is planarized by coating with a second insulating film (a coating layer of polyimide organic

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resin layer) formed on the first insulating film to planarize the first insulating film (53).

See Tran's Fig.5b and col.10 lines 8-32 and col.9 lines 60-64.

It would have been obvious to one of ordinary skill in the art to form the layer (14) in Hsieh's device of a single crystal silicon layer instead of polysilicon layer as taught by Tran et al. because single crystal silicon and polysilicon are common materials for forming the channel region in the thin film transistor device and they are interchangeable. It also would have been obvious to one of ordinary skill in the art to coat the first insulating film (20) in Hsieh's device with a polyimide layer as taught by Tran in order to obtain a smooth planarization layer (see Tran's col.10, lines 8-32). One of ordinary skill would have been motivated to do so because it is easier to form other element such as metalization on top of a smooth planarization interlayer insulating film than an uneven surface interlayer insulating film as shown in Hsieh's device.

Claims 5, 12, 19, 17, 31-47 and 52, are rejected under 35 U.S.C. 103(a) as being unpatentable over in view of Hsieh in view of Tran et al. and further in view of Liauh (US 5,027,185).

Hsieh and Tran teach all the limitations of claims 1-4, 6-11, 13-18, 20-26, 28-30, as shown above. However, Hsieh and Liauh do not teach that the conductor comprises a second conductive film of TiN.

Regarding claims 5, 12, 19, 27, 31-35, 52, Liauh discloses a semiconductor device having electrodes connected to source/drain regions (3) comprise a first

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conductive film (11, an Al layer) and a second conductive film (10, a TiN layer) between the first conductive film and source/drain regions. See Liauh's Fig.8.

It would have been obvious to one of ordinary skill in the art to form the electrode of double layer TiN/Al as taught by Liauh because TiN layer acts as a barrier layer to prevent the migration of Al layer into the silicon source /drain regions which causes the junction spiking. See Liauh's col.2, lines 44-49.

Regarding claims 36-41, as above the electrode is formed of a TiN layer under an Al layer, therefore it is inherent that the TiN is interposed between the pixel electrode and the Al layer.

Regarding claims 42-47, as shown in Hsieh's Fig.8, another electrode formed the same material as the electrode connected to another source/drain region.

### ***Response to Arguments***

3. Applicant's arguments with respect to claims 1-47 have been considered but are not persuasive.

Applicants argue that in claims there are no limitation "single crystal silicon layer" (crystalline silicon layer). In responses, claims 2, 9, 16, 24, 32, 37, 43, 49 contain, limitaion "crystalline silicon".

Applicants argue that Tran cannot combine to Hsieh because Tran does not teach the pixel electrode. In response, the limitations incorporating in Hsieh 's device does not including "pixel electrode". It is noted that the test for obviousness is not

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whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art.

See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

### ***Conclusion***

**4. Papers related to this application may be submitted to Technology center (TC) 2800 by facsimile transmission. Papers should be faxed to TC 2800 via the TC 2800 Fax center located in Crystal Plaza 4, room 4-C23. The faxing of such papers must conform with the notice published in the Official Gazette, 1096 OG 30 (November 15, 1989). The Group 2811 Fax Center number is (703) 308-7722 and 308-7724. The Group 2811 Fax Center is to be used only for papers related to Group 2811 applications.**

**5. Any inquiry concerning this communication or any earlier communication from the Examiner should be directed to CUONG Q NGUYEN whose telephone number is (703) 308-1293. The Examiner is in the Office generally between the hours of 6:30 AM to 5:00 PM (Eastern Standard Time) Monday through Thursday.**

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor TOM THOMAS who can be reached on (703) 308-2772. The fax phone

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number for the organization where this application or proceeding is assigned is (703)  
308-7722 or 308-7724.

Any inquiry of a general nature or relating to the status of this application should  
be directed to the Technology Center Receptionists whose telephone number is 308-  
0956.

CN

August 23, 2002

CUONG QUANG NGUYEN

A handwritten signature in black ink, appearing to be 'CQ' or 'CQNG', written below the printed name.